An Iterative Method for Model Order Reduction of Parasitic Resistive Networks

Suzanne Shontz
University of Kansas
shontz@ku.edu

Odile Marcotte
University of Quebec at Montreal
Odile.Marcotte@gerad.ca

Wil Schilders
Eindhoven University of Technology
w.h.a.schilders@tue.nl

Abstract

Very-large-scale integration (VLSI) chips that are manufactured today combine thousands to billions of components in an integrated circuit on a single chip. Coupling effects between the various components play a large role in chip performance and hence must be thoroughly investigated during the design phase. In order to analyze these effects, co-simulation of the nonlinear circuits and extracted parasitics is performed. Because full-device parasitic simulations are either too costly or impossible, reduced order models are sought for the parasitics, which can reproduce the behavior of the original circuit when re-coupled to the device.

In [1], the authors, along with collaborator, Petko Kitanov, developed a vertex cut algorithm for model order reduction of parasitic networks based on the graph theory concept of a vertex cut. The algorithm and its four variants described in the paper reduced the number of edges in the networks by nearly 75 to 80 percent for the electronic circuits considered. In addition, for nearly all circuit components, the number of edges in the reduced network produced by the algorithm of Lenaers described in [2] is greater than the smallest number of edges produced by any of the algorithm variants.

In our current work, we develop an iterative method for model order reduction of parasitic networks. The algorithm reduces the network by removing the resistor which least effects the network's path resistance on each iteration. Seeking further reduction of the parasitic resistive networks investigated in [1], we apply our proposed method to the reduced networks in the paper and compare our results with those in [1] and [2].

References

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