Many Core Acceleration of the Boundary Element Method

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Abstract

The Intel Xeon Phi coprocessors provide an efficient tool for the acceleration of scientific codes. Contrary to the GPGPU programming, where the code has to be adapted to the hardware design of the graphics cards, the Intel's MIC (many integrated core) technology allows for easy porting of the standard CPU code. One of the options to utilize the Xeon Phi coprocessor is to run the code on the CPU host and offload the computationally intensive parts to the coprocessor by using the Intel's offload pragmas or the offload features of OpenMP 4. To fully exploit the hardware structure of Xeon Phi it is usually necessary to optimize the offloaded kernels for aligned memory access, loop collapsing and vectorization, etc.

The BEM4I library currently utilizes the coprocessors for the assembly of the boundary element system matrices for the 3D Laplace and Lamé equations. We present the results of numerical experiments carried out on the Salomon cluster installed at the IT4Innovations NSC. With its 864 Xeon Phi 7120P cards it is the biggest Intel's installation of its many core technology in Europe. The experiments include the full assembly of BEM matrices and preliminary results for the sparsification by the ACA method. We also provide benchmarks for the boundary element tearing and interconnecting method achieved in cooperation with the developers of the domain decomposition Espreso library.

References

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